Performance Impact of Instruction Set Architecture Extensions for Dynamic Task Scheduling Units

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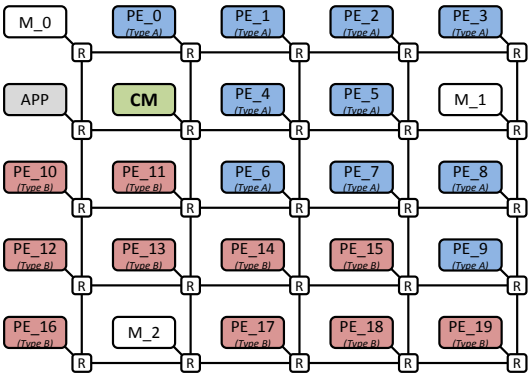


Fig. 1. Hardware system model.

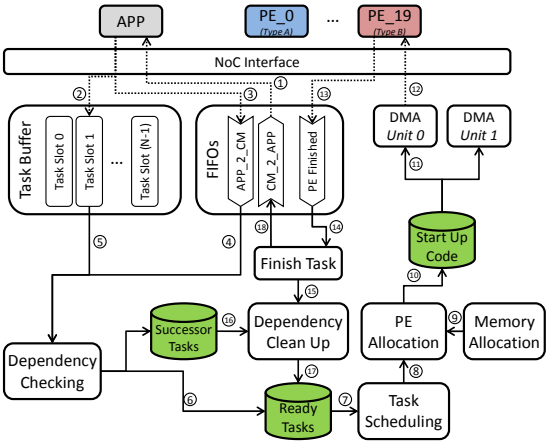


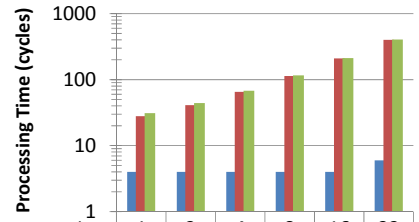
Fig. 2. CoreManager behavior

Introduction

A heterogeneous MPSoC is controlled by a dynamic task scheduling unit called CoreManager (CM). The instruction set architecture of this unit has been extended to improve performance for dynamic data dependency checking, task scheduling, processing element (PE) allocation and data transfer management [1].

Approach

The MPSoC depicted in Fig. 1 consists of 22 cores and three global memory ports (M). The data plane is composed of 20 PEs. Altogether ten digital signal processors (DSP) and ten general purpose (GP) cores are integrated. The CoreManager controls the data plane dynamically, according to the current system status. The heterogeneous nature of the system as well as the integrated local memories are considered. Its performance is improved by an application-specific instruction set, e.g., single instruction multiple data operations (SIMD). An application processor hosts the operating system and executes the sequential part of an application. All modules are connected by a 5x5 Network-on-Chip (NoC). Each module has a dedicated router, connected to its neighbors by point-to-point data links. The routers are responsible for packet scheduling and arbitration. XY routing is applied. All modules as well as the NoC are integrated in a cycle-accurate Tensilica XTSC simulation environment. Further tools have been newly developed for visualization of task executions and data transfers (TaskVisualizer [2]), as well as system status observation (DebugVisualizer [1]).



#Tasks	1	2	4	8	16	32
CM-EIS	4	4	4	4	4	6
CM-VLIW	28	41	65	113	209	401
CM-LX4	31	44	68	116	212	404

Fig. 3. Dynamic task scheduling processing time

Basic components and data flow (Fig. 2)

1-4	Task description transfer
5	Dynamic dependency check
6-7	Task scheduling
8	PE allocation
9	Memory allocation
10	PE start up code
11	DMA transfer
12-13	Task execution
14-16	Task clean up
17	Successor tasks

Results

In Fig. 3, the processing time of the task scheduling is shown. The number of tasks in the ready list are varied between 1 and 32. Three different CoreManager approaches are analyzed and compared. The CoreManager with extended instruction set (CM-EIS) outperforms the RISC-based implementations (CM-LX4 and CM-VLIW) by nearly two orders of magnitude in the case of 32 tasks. Further results can be found in [1], [3], [4] and [5]. It is faster than an ARM9-based implementation presented in [2] and [6]. Furthermore, the CoreManager CM-EIS was integrated in a TSMC 65 nm LP-CMOS prototype [7].

References

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