AIDA: Analog Integrated Circuit Design Automation

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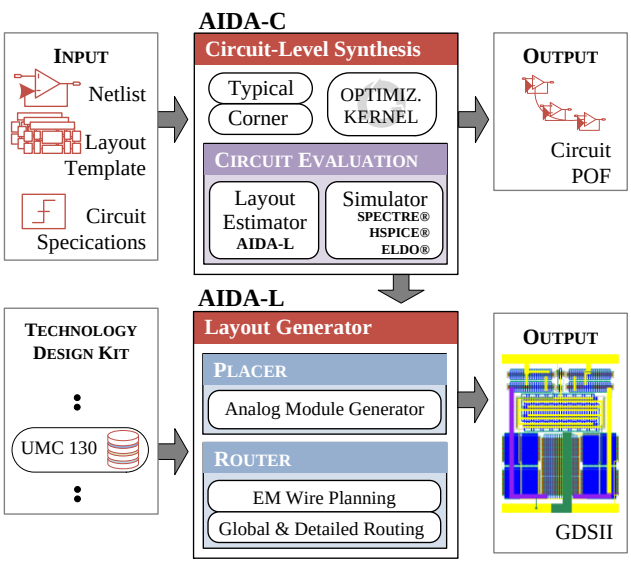
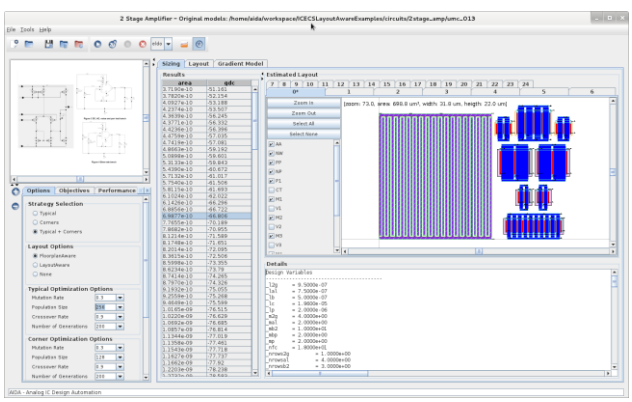
AIDA is an analog integrated circuit design automation framework, which includes two main modules: **AIDA-C** and **AIDA-L**. **AIDA-C** is a circuit-level synthesis tool supported by state-of-the-art multi-objective optimization kernels, where the robustness of the solutions is attained by considering extreme process variations by means of PVT corner analysis. The circuit's performance is measured using Spectre®, Eldo® or HSPICE® electrical simulators. **AIDA-L** considers the obtained device sizes to generate the complete layout by placing and, routing the devices, while fulfilling the technology design rules by using built-in DRC and LVS procedures, taking into account the circuit's currents to mitigate electromigration and IR-drop effects. The framework also includes a technology-independent module generator, capable of creating several simple and complex device structures/layout styles that allow the **AIDA-C** floorplan-aware optimizer to explore a much wider space of solutions and to produce higher quality layouts. **AIDA** is demonstrated for different classes of circuits, such as, OpAmps, LNAs, LC-VCOs, etc. for both circuit and layout level synthesis.



Graphical User Interface

AIDA includes an intuitive GUI for managing the implemented design flow with inputs and outputs from/to major commercial IC design tool sets.



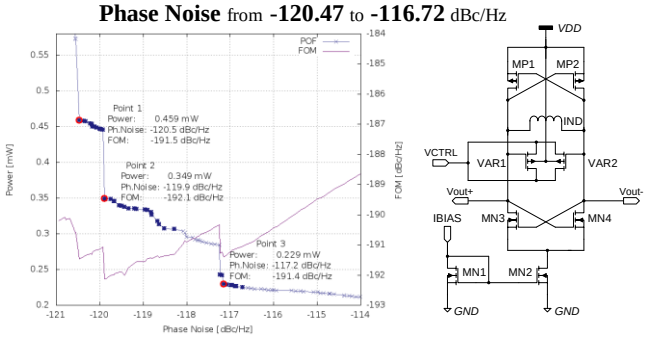
2.4 GHz LC-VCO

Multi-Objective Multi-Constraint Circuit-Level Synthesis

Objectives: **minimize Power Consumption** and **Phase Noise**

Constraints: **Phase Noise** ≤ **-100** dB, **Power Consumption** ≤ **6** mW
Output Voltage Swing ≥ **100** mV
2.4 GHz ≤ **Oscillating Frequency** ≤ **2.4835** GHz
Overdrive voltage ≥ **80** mV; **Saturation** margin ≥ **50** mV

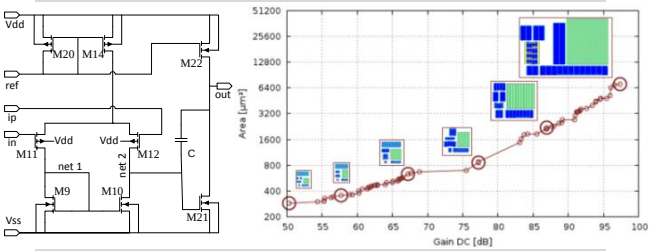
Results: **40 State-of-the-Art Solutions (FOM** ≤ **-191** dBc/Hz **)**
Power Consumption from **0.22** to **0.46** mW
Phase Noise from **-120.47** to **-116.72** dBc/Hz



Two-stage OpAmp

Objectives: **min. area** and **max. dc gain**
Multiple Layout Templates

Layout-Aware Circuit-Level Synthesis



Electromigration-Aware Layout Generation